2111A

256 x 4 STATIC RAM

2111A-2	250 ns Max.
2111A	350 ns Max.
2111A-4	450 ns Max.

- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 18 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150 mW**
- **Three-State Output: OR-Tie Capability**

The Intel® 2111A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

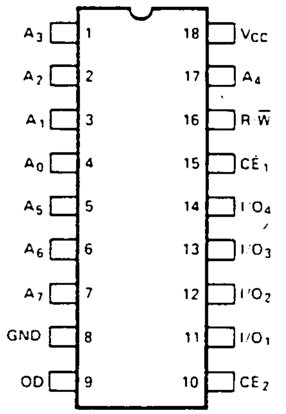
The 2111A is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

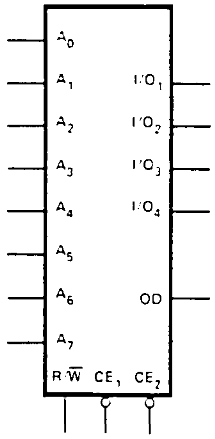
The Intel® 2111A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

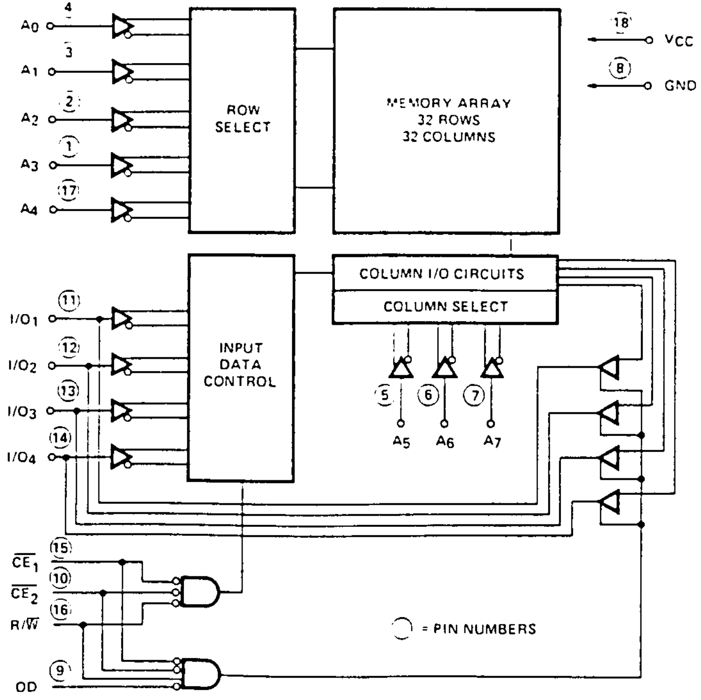
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/$\overline{W}$	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
CE_2	CHIP ENABLE 2
I/O_1-I/O_4	DATA INPUT/OUTPUT

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . -0.5V to +7V

Power Dissipation . . . . 1 Watt

COMMENT:

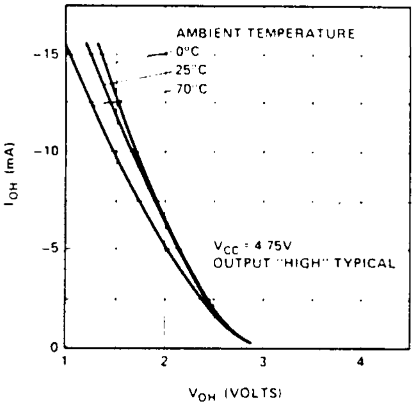
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

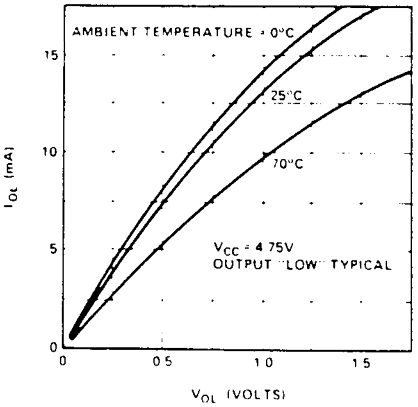
T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current		1	10	μA	Output Disabled, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current		-1	-10	μA	Output Disabled, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current 2111A, 2111A-4		35	55	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 25°C
	2111A-2		45	65		
I_{CC2}	Power Supply Current 2111A, 2111A-4			60	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 0°C
	2111A-2			70		
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage 2111A, 2111A-2	2.4			V	I_{OH} = -200μA
	2111A-4	2.4			V	I_{OH} = -150μA

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2111A-2 (250 ns ACCESS TIME)

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			250	ns	
t_{CO}	Chip Enable To Output			180	ns	
t_{OD}	Output Disable To Output			130	ns	
t_{DF} [3]	Data Output to High Z State	0		180	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

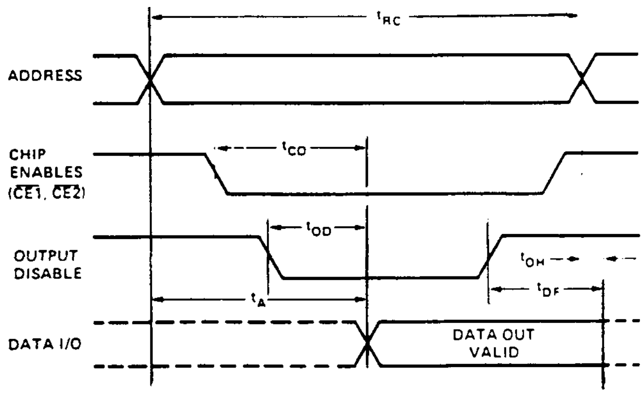
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	150			ns	
t_{DW}	Data Setup	150			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	150			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

CAPACITANCE[2] T_A = 25°C, f = 1 MHz

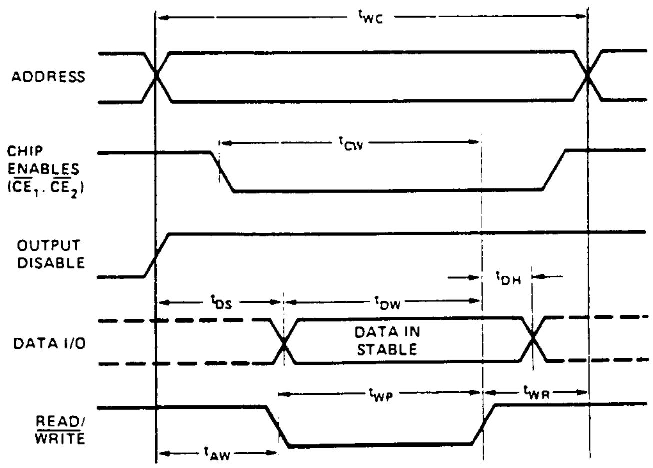
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.